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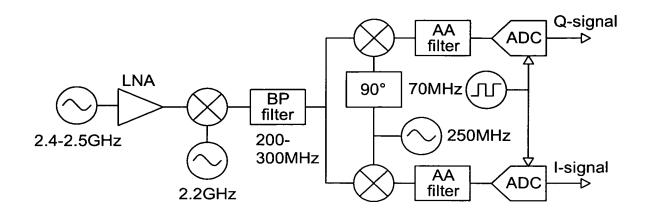


FIG. 1

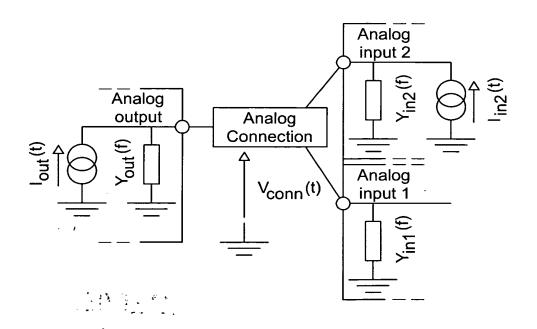
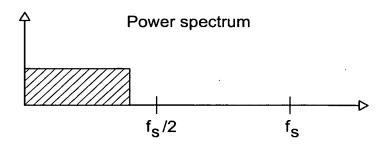


FIG. 2



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Baseband representation



Equivalent low-pass representation

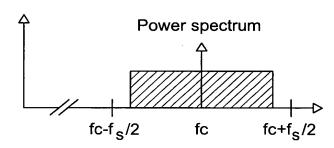


FIG. 3

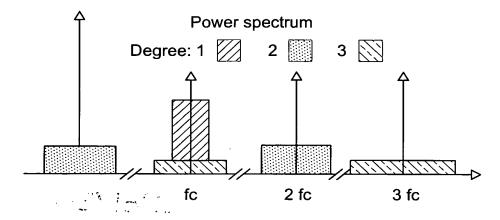


FIG. 4



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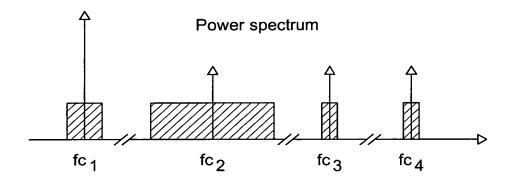


FIG. 5

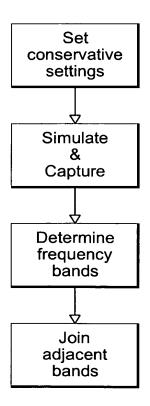


FIG. 6

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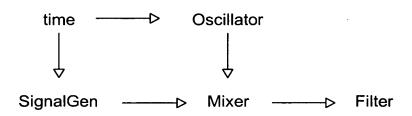
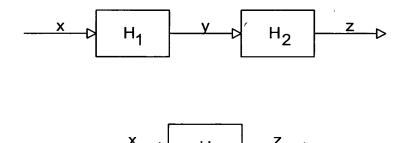


FIG. 7



 $H = cascade (H_1, H_2)$

FIG. 8

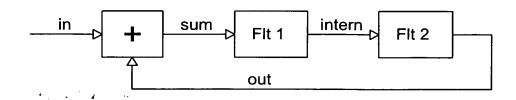


FIG. 9



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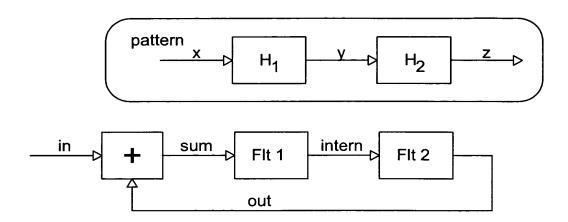


FIG. 10

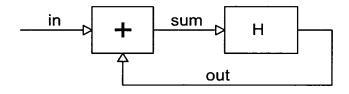


FIG. 11

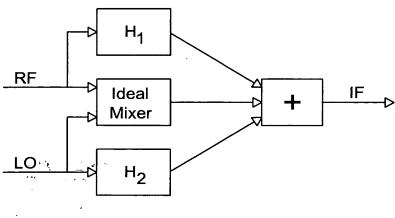


FIG. 12

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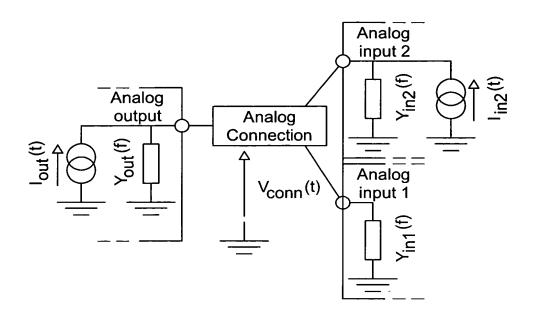


FIG. 13

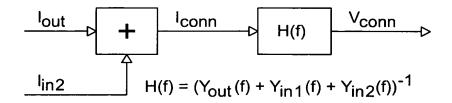
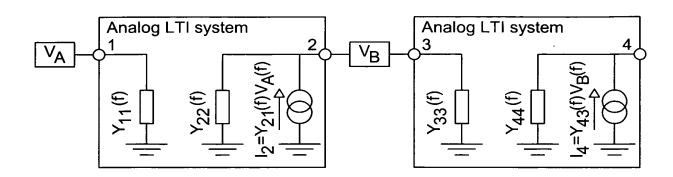


FIG. 14



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$$V_{A} > V_{21}(f)$$
 $V_{B} > V_{43}(f)$ $V_{43}(f)$ $V_{43}(f)$

FIG. 15

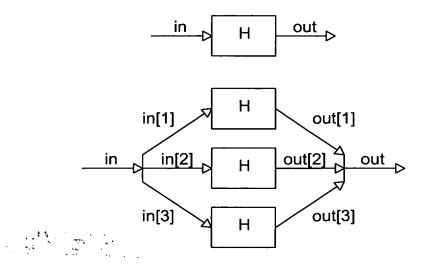
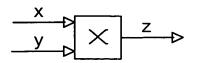


FIG. 16





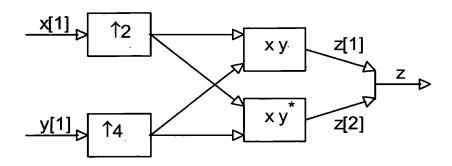


FIG. 17

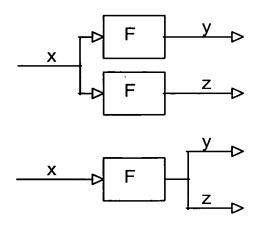
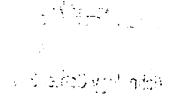


FIG. 18





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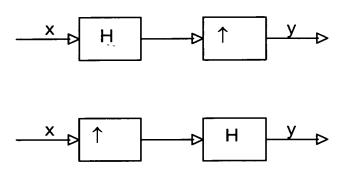


FIG. 19

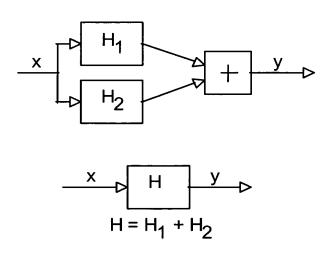


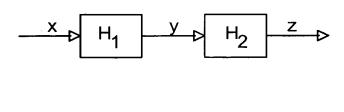
FIG. 20



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 $H = cascade (H_1, H_2)$

FIG. 21

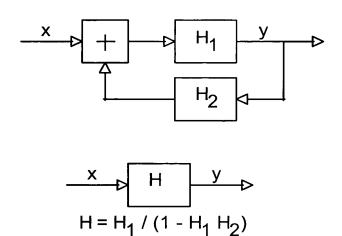


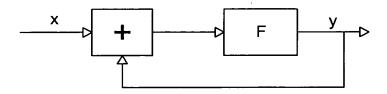
FIG. 22

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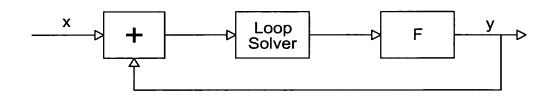
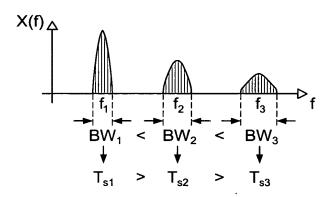


FIG. 23



Spectral representation of an MRMC signal

FIG. 24

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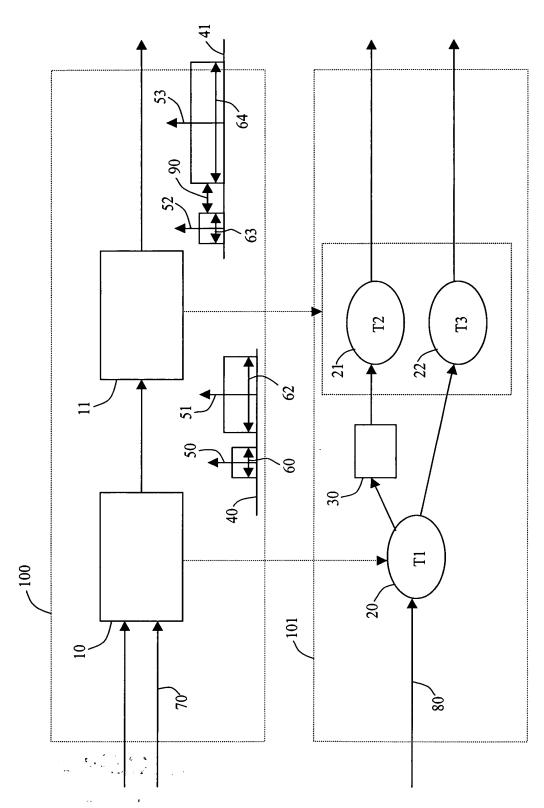


FIG. 25



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ary Simulation representations representations ur subcircuits y of nodes y of nodes d Computation Rules								
Input Circuit (grapl Perform Prelimin Determine signal Simplify signal Construct Comp in pluralit in pluralit Executed Schedule	Input Circuit (graphical, text format)	Perform Preliminary Simulation	Determine signal representations	Simplify signal representations	Construct Computational graph	Add up/down sampling nodes Split linear subcircuits in plurality of nodes method for nonlinear circuits	Scheduling of computation nodes - preferring vector processing modes	Executed Scheduled Computation Rules
Input Circuit Perform Pre Determine is Simplify simpling nodes Construct in ping uling of computation	Input Circuit	Perform Pre	Determine s	Simplify s	Construct (Scheduling of computation	Executed Sche

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Node 1 Node 2 Node 3